Hardware/Software Codesign Lab Requirements

1. Follow the Lab 2 manual finish Lab 2. Test the lab on board and demonstrate it to instructor.
2. Upload the following documents to Beachboard Lab 2 submission link:
3. PDF file of the completed design for your hardware platform, see Figure 15 in Lab 2 Manual.
4. Excel spreadsheet for peripheral memory map, see Figure 14 in Lab 2 Manual.
5. system.mss file
6. system.hdf

Note: Both the PDF file and the Excel file can be generated by right click the source and save it to the required format within Vivado IP Integrator.

1. Answer the following questions below, attach your answer to the end of this document and submit this document:
2. **List the major operations in Steps 2 & 3 in Lab 2 manual.**

* Enable AXI\_M\_GP0 interface, FCLK\_RESET0\_N, and FCLK\_CLK0 ports, Add two instances of a GPIO Peripheral from the IP catalog to the processor system
* The push button and dip switch instances will be connected to corresponding pins on the board. This can be done manually or using Designer Assistance. Normally, one would consult the board’s user manual to find this information.

1. **At which step the Vivado tool generates xparameter.h? Does Lab 1 and Lab 2 have the same xparameter.h? If different, Please describe the major difference. If the same, explain why.**

* In Step 5. Specifically Step 5-1-9, in which the library generator runs in the background creating the xparameter.h. We did not have this file in lab 1.

1. **What is the difference between Lab 1 and Lab 2 when we export hardware platform from Vivado IP integrator to SDK?**

* We included the bitstream in Lab 2, but not in Lab 1.

1. **Describe the difference between Lab 1 and Lab 2 for running the application program.**

* The difference I noticed was that we had to program the FPGA first before running the Programming System in lab 2, where as in Lab 1, we didn’t program the FPGA.